WHAT IS CLAIMED IS:

1. A semiconductor device comprising first, second, third and fourth resistor elements, the first to fourth resistor elements having first ends commonly connected to a first node, and operating in one of first and second operation modes which are switchable,

wherein the first and second resistor elements include second ends connected to a second node and a third node, respectively,

the third and fourth resistor elements include second ends connected to a fourth node and a fifth node via a first switch and a second switch, respectively,

the first and second switches are opened in the first operation mode, and

the first and second switches are closed in the second operation mode.

2. The semiconductor device according to claim 1, wherein a first voltage is applied between the second node and the third node, and a voltage substantially equal to the first voltage is applied between the fourth node and the fifth node in the second operation mode.

3. The semiconductor device according to claim 1, wherein a resistance value of the first resistor element and a resistance value of the second resistor element are substantially equal, and a resistance value of the third resistor element and a resistance value of

the fourth resistor element are substantially equal.

4. The semiconductor device according to claim 1, wherein a ratio between a resistance value of the first resistor element and a resistance value of the second resistor element is substantially equal to a ratio between a resistance value of the third resistor element and a resistance value of the fourth resistor element.

5. The semiconductor device according to claim 1, wherein the first to fourth resistor elements are formed on a major surface of a semiconductor substrate, and a parasitic capacitance of the third resistor element is substantially equal to a parasitic capacitance of the fourth resistor element.

6. The semiconductor device according to claim 1, wherein a resistance value of the third resistor element and a resistance value of the fourth resistor element are lower than a resistance value of the first resistor element and a resistance value of the second resistor element.

7. A semiconductor device comprising:

an output adjusting circuit which includes a first input terminal supplied with a fixed potential, a second input terminal supplied with a reference potential from a reference node, and an output terminal, and is operable in a standby mode and in an active mode; and an output setting unit including a first output setting circuit connected between the reference node and a reference potential terminal, and a second output setting circuit connected between the output terminal and the reference node,

wherein the first output setting circuit includes at least first and second resistor elements connected in series via a first voltage-division node between the reference node and the reference potential terminal in the standby mode, and at least third and fourth resistor elements connected in series via a second voltage-division node connected to the first voltage-division node between the reference node and the reference potential terminal in the active mode, and a ratio in resistance value between the first resistor element and the second resistor element is substantially equal to a ratio in resistance value between the third resistor element and the fourth resistor element, and

the second output setting circuit includes at least fifth and sixth resistor elements connected in series via a third voltage-division node between the output terminal and the reference node in the standby mode, and at least seventh and eighth resistor elements connected in series via a fourth voltage-division node connected to the third voltage-division node between the output terminal and the reference node in the active mode, and a ratio in resistance value between the fifth resistor element and the sixth resistor element is substantially equal to a ratio in resistance value between the seventh resistor element and the eighth resistor element.

8. The semiconductor device according to claim 7, wherein the output setting unit includes an n-number of output setting circuits containing a first output setting circuit to an n-th output setting circuit (n: a natural number, n ≧ 2), and

the n-th output setting circuit includes at least a (4n-3)-th resistor element and a (4n-2)-th resistor element connected in series via a (2n-1)-th voltage-division node between the output terminal and the reference node in the standby mode, and at least a (4n-1)-th resistor element and a 4n-th resistor element connected in series via a 2n-th voltage-division node connected to the (2n-1)-th voltage-division node between the output terminal and the reference node in the active mode, and a ratio in resistance value between the (4n-3)-th resistor element and (4n-2)-th resistor element is substantially equal to a ratio in resistance value between the (4n-1)-th resistor element and 4n-th resistor element.

9. The semiconductor device according to claim 7, wherein the output adjusting circuit includes a comparison circuit that compares the reference

potential from the reference node and the fixed potential, and a control element that controls an output current to be supplied to the output terminal in accordance with an output from the comparison circuit.

10. The semiconductor device according to claim 7, wherein the first to eighth resistor elements are formed on a major surface of a semiconductor substrate,

a parasitic capacitance of the first resistor element is substantially equal to a parasitic capacitance of the second resistor element,

a parasitic capacitance of the third resistor element is substantially equal to a parasitic capacitance of the fourth resistor element,

a parasitic capacitance of the fifth resistor element is substantially equal to a parasitic capacitance of the sixth resistor element, and

a parasitic capacitance of the seventh resistor element is substantially equal to a parasitic capacitance of the eighth resistor element.

11. The semiconductor device according to claim 8, wherein the (4n-3)-th to 4n-th resistor elements are formed on a major surface of a semiconductor substrate,

a parasitic capacitance of the (4n-3)-th resistor element is substantially equal to a parasitic capacitance of the (4n-2)-th resistor element, and

a parasitic capacitance of the (4n-1)-th resistor element is substantially equal to a parasitic capacitance of the 4n-th resistor element.

12. The semiconductor device according to claim 10, wherein the semiconductor substrate is of a P-type, and the first to eighth resistor elements are formed of N-type impurity regions diffused on the P-type semiconductor substrate.

13. The semiconductor device according to claim 11, wherein the semiconductor substrate is of a P-type, and the first to 4n-th resistor elements are formed of N-type impurity regions diffused on the P-type semiconductor substrate.

14. The semiconductor device according to claim 10, wherein the semiconductor substrate is of an N-type, and the first to eighth resistor elements are formed of P-type impurity regions diffused on the N-type semiconductor substrate.

15. The semiconductor device according to claim 11, wherein the semiconductor substrate is of an N-type, and the first to 4n-th resistor elements are formed of P-type impurity regions diffused on the N-type semiconductor substrate.

16. The semiconductor device according to claim 7, wherein the first, second, fifth and sixth resistor elements have higher resistance values than the third, fourth, seventh and eighth resistor elements, respectively.

17. The semiconductor device according to claim 7,

wherein the first and second resistor elements have substantially equal resistance values, the third and fourth resistor elements have substantially equal resistance values, the fifth and sixth resistor elements have substantially equal resistance values, and the seventh and eighth resistor elements have substantially equal resistance values.

18. The semiconductor device according to claim 17, wherein the first to eighth resistor elements are formed of diffusion layers which are formed by diffusing impurities of a second conductivity type in a semiconductor substrate of a first conductivity type, the diffusion layers of the first and second resistor elements have substantially equal areas, the diffusion layers of the third and fourth resistor elements have substantially equal areas, the diffusion layers of the fifth and sixth resistor elements have substantially equal areas, and the diffusion layers of the seventh and eighth resistor elements have substantially equal areas.

19. The semiconductor device according to claim 10, wherein the third and fourth resistor elements and the seventh and eighth resistor elements are connected between the output terminal and the reference potential terminal via switches that are turned on in the active mode, and the switches are formed of NMOS transistors formed in the P-type

semiconductor substrate.

20. The semiconductor device according to claim 10, wherein the third and fourth resistor elements and the seventh and eighth resistor elements are connected between the output terminal and the reference potential terminal via switches that are turned on in the active mode, and the switches are formed of PMOS transistors formed in the N-type semiconductor substrate.

21. The semiconductor device according to claim 10, wherein the third and fourth resistor elements and the seventh and eighth resistor elements are connected between the output terminal and the reference potential terminal via switches that are turned on in the active mode, and each of the switches includes an NMOS transistor and a PMOS transistor connected in parallel and formed on the semiconductor substrate.

22. A semiconductor device comprising:

a first power supply terminal and a second power supply terminal;

a first charging circuit having one end connected to the first power supply terminal and the other end connected to one end of a resistor element;

a discharging circuit having one end connected to the other end of the resistor element, and the other end connected to the second power supply terminal;

a capacitor having one end connected to said one end of the resistor element, and the other end connected to the second power supply terminal; and

a second charging circuit having one end connected to the first power supply terminal, and the other end connected to said other end of the resistor element.

23. The semiconductor device according to claim 22, wherein the first power supply terminal is a positive power supply terminal, the second power supply terminal is a ground terminal, each of the first and second charging circuits includes a PMOS transistor, and the discharging circuit includes an NMOS transistor.

24. The semiconductor device according to claim 22, further comprising a third charging circuit having one end connected to the first power supply terminal, and the other end connected to a middle point of the resistor element.

25. The semiconductor device according to claim 22, further comprising a plurality of auxiliary charging circuits each having one end commonly connected to the first power supply terminal, and the other end connected to an associated one of a plurality of intermediate points of the resistor element.

26. The semiconductor device according to claim 22, wherein the first power supply terminal is a ground terminal, the second power supply terminal is a

positive power supply terminal, each of the first and second charging circuits includes an NMOS transistor, and the discharging circuit includes a PMOS transistor.

27. The semiconductor device according to claim 26, further comprising a third charging circuit that includes an NMOS transistor having one end connected to the first power supply terminal, and the other end connected to a middle point of the resistor element.

28. The semiconductor device according to claim 27, further comprising a plurality of auxiliary charging circuits that include NMOS transistors each having one end connected to the first power supply terminal, and the other end connected to an associated one of a plurality of intermediate points of the resistor element.

29. The semiconductor device according to claim 22, wherein the first charging circuit and the second charging circuit include substantially equal driving performances.